UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,619	12/30/2003	David M. Puffer	42P17994	8290

7590 05/01/2006

EXAMINER
PATEL, NITIN C

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/01/2006

John P. Ward
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,619	PUFFER ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/04 and 1/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to communication filed on 13 January 2006.

2. Claims 1 – 16 are presented for the examination.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 6 May 2004, and 13 January 2006 were filed before the mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 7, and 12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Cho et al. [hereinafter as Cho], US Patent 6,021,506 B1.

5. As to claims 1, 7, and 12, Cho discloses a method, comprising:

a. receiving an electrical idle ordered set [to stop iclk, internal clock] at a receiving device power management unit [col. 5, lines 52 – 55, fig. 3];

b. entering a low power entry state [with iclk stopped] if there is no activity [does not detect any receive activity] on an interconnect when the electrical idle ordered set [MOD_RUN low] is received [col. 5, lines 66 – 67, col. 6, lines 1 – 6]; and

c. bypassing [objection to stopping] the low power entry state [with iclk stopped] and entering a low power reset state [iclk continue to run] if there is activity on the interconnect when the electrical idle ordered set is received [col. 5, lines 52 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 2, fig. 3 – 5].

6. Claims 1 – 16 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yu et al. [hereinafter as YU], US Patent 6,463,541 B1.

7. As to claim 1, Yu discloses a method, comprising:

a. receiving an electrical idle ordered set [receive system activity idle, buffer empty indicator, an idle indicator] at a receiving device power management unit [68, power management mechanism, fig. 2 – 3];

b. entering a low power entry state [power-down mode] if there is no activity [does not detect any receive activity] on an interconnect [network] when the electrical idle ordered set [an idle indicator] is received [col. 4, lines 19 – 25, and 58 – 67]; and

c. bypassing [as shown in step 308 when RX_Idle bit is not equal to one] the low power entry state [power-down mode] and entering a low power reset state [operation mode] if there is activity on the interconnect when the electrical idle ordered set is received [col. 4, lines 19 – 67, col. 5, lines 30 – 58, fig. 2 – 3].

8. As to claim 7, Yu discloses an apparatus [fig. 1A, 2] comprising:

a. a receiver circuit [26a, MAC RX block] to provide electrical connection to an interconnect [fig. 2];

b. an interconnect activity check unit [206 receive idle indicator] coupled to the receiver circuit, the interconnect activity check unit to determine whether there is activity on the interconnect [to check network activity] [col. 4, lines 60 – 63];

c. a pipeline to process [CPU process SRAM receive buffer] incoming signals received at the receiver circuit [col. 4, lines 8 – 18]; and

d. a power management unit [68, power management indication] to turned off [power down] the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management unit if the interconnect activity check unit [206, receive idle indicator] indicates that there is no activity on the interconnect [no network activity][col. 4, lines 58 – 67, col. 5, lines 30 – 48], and the power management unit to not turn off [continue to the operation (i.e. not powered down)] the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management unit if the interconnect activity check unit indicates that there is activity of the interconnect [col. 5, lines 49 – 58, fig. 2 – 3].

9. As to claim 12, Yu discloses a system, comprising:

a. a transmitting device [26b, MAC TX block, fig. 2]; and

b. a receiving device [26a, MAC RX block] coupled to the transmitting device via an interconnect [fig. 1A, 2], the receiving device including a receiver circuit to provide electrical connection to the interconnect, an interconnect activity check unit [206, receive idle indicator] coupled to the receiver circuit, the interconnect activity check unit [206, receive idle indicator] to determine whether there is activity on the interconnect [to check network activity] [col. 4, lines 60 – 63], a pipeline to process

incoming signals received at the receiver circuit[col. 4, lines 8 – 18], and a power management unit to turn off the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management unit if the interconnect activity check unit indicates that there is no activity on the interconnect[no network activity][col. 4, lines 58 – 67, col. 5, lines 30 – 48], and the power management unit to not turn off [continue to the operation (i.e. not powered down)] the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management uniit if the interconnect activity check unit indicates that there is activity [col. 5, lines 49 – 58, fig. 2 – 3] of the interconnect [abstract, col. 1, lines 39 – 48, 56 – 67, col. 2, lines 1 – 5, 40 – 65, col. 3, lines 23 – 67, col. 4, lines 1 – 67, col. 5, lines 1 – 58, fig. 1a, 2, and 3].

10. As to claim 2, Yu discloses entering a low power entry state [power-down mode], which inherently teaches turning off a receiver circuit in the receiving device [18a, fig. 1a, 2].

11. As to claim 3, Yu discloses power management operations of system performed by CPU to reduce power consumption including different modes e.g. power-down mode, a magic packet mode including entering a low power idle state following the low power state [col. 5, lines 7 – 53].

12. As to claim 4, Yu teaches exiting the low power idle state [power-down mode] and entering in the low power receiver on state [operation mode] when activity is detected [receive idle indicator is not one] on the interconnect [network] col. 5, lines 49 – 54, fig. 3].

13. As to claim 5, Yu teaches the low power idle state [power-down mode] and entering in the low power receiver on state [operation mode] including turning on receiver circuit [18a] when activity is detected [receive idle indicator is not one] on the interconnect [network] [col. 5, lines 49 – 54, fig. 3].

14. As to claim 5, Yu teaches exiting the low power idle state [power-down mode] and entering in the low power receiver on state [operation mode] including entering low power receiver reset state [col. 5, lines 7 – 54, fig. 3].

15. As to claims 8, and 13, Yu discloses network interface in accordance with PCI specification [col. 2, lines 58 – 59] including a network protocol [col. 3, lines 46 – 53] including the pipeline [SRAM buffer], which inherently teaches including data extraction unit [66 CPU] and a packet processing unit [66 CPU][fig. 2].

16. As to claims 9, and 14, Yu discloses a receiver circuit including a pair of inputs to receive a pair of differential signals [TXD+/-, RXD+/-], the differential signals included as part of the interconnect [fig. 1b].

17. As to claims 10, and 15, Yu discloses an interconnect activity check unit [204, transmit idle indicator, 206, receive idle indicator, fig. 2a] to indicate [check] there is no activity on interconnect [network] including a differential pair of signals [TXD+/-, RXD+/-] at approximately common mode voltage.

18. As to claims 11, and 16, Yu discloses network interface in accordance with PCI specification revision 2.1 [col. 2, lines 58 – 59] which includes a PCI Express interconnect.

19. Claims 1, 7, and 12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Cho et al. [hereinafter as Cho], US Patent 6,021,506 B1.

20. As to claims 1, 7, and 12, Cho discloses a method, comprising:

a. receiving an electrical idle ordered set [to stop iclk, internal clock] at a receiving device power management unit [col. 5, lines 52 – 55, fig. 3];

b. entering a low power entry state [with iclk stopped] if there is no activity [does not detect any receive activity] on an interconnect when the electrical idle ordered set [MOD_RUN low] is received [col. 5, lines 66 – 67, col. 6, lines 1 – 6]; and

c. bypassing [objection to stopping] the low power entry state [with iclk stopped] and entering a low power reset state [iclk continue to run] if there is activity on the interconnect when the electrical idle ordered set is received [col. 5, lines 52 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 2, fig. 3 – 5].

21. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

22. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
April 25, 2006

A. ELAMIN
PRIMARY EXAMINER